★★★　＜知的財産翻訳検定＞答案用紙　★★★

科　　目：電気電子工学

氏　　名：中村真理子

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※以下に解答を記入してください

1

VOLUME CONTROL CIRCUIT AND VOLUME CONTOLLING METHOD USED FOR PORTABLE CAR TELEPHONE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The prenset invention relates to a volume control circuit, and in particular, to a volume control circuit which is used for equipment such as a car telephone in which the installation location thereof is changeable, that is, a portable car telephone for example.

RELATED ART

Portable car telephones may be used by being installed in cars or be used by being carried. In order to enable speaking in the optimum volume corresponding to the respective environments when used on vehicle and when used by being carried,

a car telephone usually includes a volume control circuit. More specifically, when a car telephone is used on vehicle, the volume is set larger since the enviromental noise is large. On the other hand, when it is used by being carried, the volume is set smaller since the environmental noise is small. However, a conventional volume control circuit requires a volume adjustment each time the used condition is changed as described above. Therefore, the telephone causes troubles when used for speaking, and is inconvenient in use.

In vew of the aforementioned situation, an object of the present invention is to provide a volume control circuit wiht a high usability.

Another object of the present invention is to provide a volume control circuit not requiring a volume adjustment each time the used condition of the equipment is changed.

WHAT IS CLAIMED IS:

1. A volume control circuit comprising:

means for amplifying a volume signal;

first and second retention means for retaining a gain of the means for amplifying at first and second prescribed values, respectively;

state detecting means for detecting a used state of equipment into

which the volume control circuit is incorporated, and outputting

a state detection signal; and

switching means for enabling either of the first and second retaining means corresponindg to the state detection signal.

2. The volume control circuit as claimed in claim 1, further comprising, setting means for selectively changing first and second set values of the first and second retaining means corresponding to the state detection signal.

3. A volume controlling method comprising the steps of:

retaining a plurality of amplification factors corresponding to a plurlaity of used states of equipment, respectively;

detecting any of the plurality of used states, and outputting a state detection signal; and

selecting any of the plurality of amplification factors corresponding to the state detection signal, and amplifying a volume signal.

4. The volume controlling method as claimed in claim 3, further comprising a step of changing the plurality of amplification factors by hand.

2.

Hereinafter, the operation of the pulse detecting circuit will be described. When a clock pulse to the input terminal CLK takes a Vdd level, the FETs T3 and T5 are disconnected and the FETs T4 and F6 are conducted. Therefore, a Vss level is applied to either end of the capacity C3. When the level of the clock pulse changes to the Vss level, the FET T3 becomes conducted, and the Vdd level is applied to one end of the capacity C3. At this time, assuming that the point D is at the Vss level, the substrate of the FET T5 takes the Vss level, whereby this FET cannot be conducted as a transistor operation. However, the electric potential of the other end of the capacity C3 increases along with a rise of the level at the one end to the Vdd level, whereby a PN junction consisting of the substrate of the FET T5 and the connecting region to the capacity C3 side is biased in a forward direction. As a result, current flows via the PN junction so as to charge the capacity C4. With a rise of potential at the point D due to the capacity C4 being charged, the FET T5 is conducted with a transistor operation, and the current flowing via the capacity C3 flows the source-drain path of the FET T5. At the same time, in the FET T5, a connecting electrode to the capacity C3 side works as a source. Since the clock pulse takes the Vss level whereby the FETs T3 and T5 are disconnected, the point D is charged to a level lower than the Vdd level.