★★★　＜知的財産翻訳検定＞答案用紙　★★★

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※以下に解答を記入してください

問１

SOUND VOLUME CONTROL CIRCUIT USED IN PORTABLE CAR-PHONE AND METHOD FOR CONTROLLING SOUND VOLUME

BACKGROUND

Technical Field

The present invention relates to sound volume control circuits, and particular to a sound volume control circuit used in a movable apparatus such as a portable car-phone.

Related Art

Portable car-phones are used in a car in some cases, and used while being carried in other cases. Typical car-phones include a sound volume control circuit in order to allow conversation with optimum sound volume suitable for environments during an in-car use mode and a carry use mode. More specifically,

during the in-car use mode, sound volume is increased since the environmental noise is large, while during the carry use mode, sound volume is decreased since the environmental noise is small. However, a conventional sound volume control circuit requires volume adjustment every time the use mode is changed as above. These adjustments lead to a labor when conversation, resulting in the unavailability of telephone usage.

In consideration of such a present condition, the present invention is intended to provide a sound volume control circuit having improved usability.

The present invention is also intended to provide a sound volume control circuit in which sound volume need not be adjusted every time the use mode of the apparatus is changed.

CLAIMS

What is claimed is:

1. A sound volume control circuit comprising:

amplification means for amplifying a sound signal;

first holding means for holding a gain of the amplification means at a first predetermined value;

second holding means for holding a gain of the amplification means at a second predetermined value;

mode detection means for detecting a use mode of an apparatus having the sound volume control circuit so as to output a mode detection signal; and

switch means for enabling either of the first holding means or the second holding means in response to the mode detection signal.

2. The sound volume control circuit according to claim 1, further comprising setting means for selectively changing first and second set values of the first and second holding means in response to the mode detection signal.

3. A method for controlling sound volume, comprising the steps of:

holding a plurality of amplification factors corresponding to a plurality of use modes of an apparatus;

detecting any of the plurality of use modes so as to output a mode detection signal;

selecting, in response to the mode detection signal, any of the amplification factors corresponding to the mode detection signal so as to amplify a sound signal.

4. The method for controlling sound volume according to claim 3, further comprising a step of manually changing the plurality of amplification factors.

問 2.

The operation of the pulse detection circuit will be described below. When a clock pulse to the input terminal CLK takes a Vdd level, the FETs T3 and T5 become a cut-off state while the FETs T4 and T6 become a conductive state. Thus a Vss level is given to the both ends of the capacitance C3. When the clock pulse turns to the Vss level, the FET T3 becomes conductive, providing one end of the capacitance C3 with the Vdd level. At this time, if the point D is at the Vss level, the substrate of the FET T5 takes the Vss level. Therefore, this FET can not flow a current due to transistor operation. However, since the potential of the other end of the capacitance C3 increases as the potential of one end of the capacitance C3 rises to the Vdd level, a PN junction between the substrate of the FET T5 and the region connecting to the capacitance C3 is forward biased. As a result, a current flows through the PN junction to charge the capacitance C4. The potential rising at the point D due to the charging of the capacitance C4 causes the FET T5 to flow a current based on transistor operation, with the result that a current via the capacitance C3 flows through the source-drain channel of the FET T5. Also, at this time, the electrode of the FET T5 connecting to the capacitance C3 serves as a source. A clock pulse takes the Vss level, and thereby the FETs T3 and T5 become a cut-off state. Thus the point D is charged to a level lower than the Vdd level.