★★★　＜知的財産翻訳検定＞答案用紙　★★★

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※以下に解答を記入してください

問１.

Title of the Invention

Sound Volume Control Circuit and Method for Use in Portable Car Phone and Like

Background of the Invention

Technical Field

The present invention relates to a sound volume control circuit, and particularly relates to a sound volume control circuit for use in a portable apparatus such as a car phone, etc.

Description of the Related Art

A portable car phone is used while it is installed in a car, and also while it is carried around. An ordinary car phone includes a sound volume control circuit so that the user can make calls at an optimum sound volume depending on the environment of use when installed in the car or when carried around. To be more specific, when installed in the car, the car phone is used with its volume increased because of big environmental noise in

the car, while when carried around it is used with the volume reduced because there is no such big noise therearound. However, conventional sound volum control circuits require volume adjustment each time the use environment is changed. This bothers users a lot when making phone calls, making them feel inconvenience in using the car phone.

In view of this situation, an object of the present invention is to provide a sound volume control circuit which is easy to use.

Another object of the present invention is to provide a sound volume control circuit which does not require sound volume adjustment each time the use environment of an apparatus is changed

What is claimed is:

1. A sound volume control circuit comprising:

means for amplifying an audio signal;

first and second holding means for holding a gain of said amplifying means at first and second predetermined values respectively;

status detecting means for detecting a usage status of an apparatus incorporating said sound volume control circuit and outputting a status detection signal;

and

switch means for enabling either said first holding means

or said second holding means in response to the status detection signal.

2. The sound volume control circuit according to claim 1, further comprising

setting means for selectively changing the first and second predetermined values of said firt and second holding means in response to the status detection sigal.

3. A sound volume control method comprising the steps of:

holding a plurality of gaings corresponding to a plurality of usage statuses of an apparatus;

detecting any of the plurality of usage statuses and outputting a status detection signal; and

selecting a corresponding one of the gains in response to the status detection signal and amplifying an audio signal with the selected gain.

4. The sound volume control method according to claim 4, further comprising the step of

changing the plurality of gains manually.

問2.

The operation of the pulse detection circuit will now be described. When the clock pulse input to the input terminal CLK is at the Vdd level, the P-channel FETT3 and T5 become electrically discontinuous whereas the N-channel FETT4 and T6 become electrically continuous, so a voltage at the Vss level

is therefore supplied to the both ends of the capacitor C2. When the clock pulse changes to the Vss level, the P-channel FETT3 becomes electrically continuous and a voltage at the Vdd level is supplied to the one end of the capacitor C3. At this time, if the node D is at the Vss level, the substrate of the P-channel FETT5 is at the level Vss. The P-channel FETT5 cannot therefore be turned on to function as a transistor. However, since the potential of the other end of the capacitor C3 increases as the one end thereof increases to the Vdd level, the PN junction formed by the substrate of the P-channel FETT5 and the region of the P-channel FETT5 connected to the capacitor C3 is biased in the normal direction. As a result, a current flows through the PN junction and the capacitor C4 is charged with the current. Increase in the potential of the node D due to the capacitor C4 being charged causes the P-channel FETT5 to function as a transistor and thereby to be turned on, making a current that passes through the capacitor C3 flow through the source-drain pasage of the P-channel FETT5. Further, at this time, the electrode of the P-channel FETT5 that connects to the capacitor C3 works as the source. When the clock pulse is at the Vss level, the P-channel FETT3 and T5 become electrically discontinuous and the node D is therefore charged to a lower level than the Vdd level.