★★★　＜知的財産翻訳検定＞答案用紙　★★★

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※以下に解答を記入してください

(問１)

TITLE OF THE INVENTION

VOLUME CONTROL CIRCUIT FOR USE IN PORTABLE AUTOMOBILE PHONE AND OTHERS AND VOLUME CONTROL METHOD

BACKGROUND OF THE INVENTION

Technical Field

The present invention relates to volume control circuits and more particularly to a volume control circuit for use in equipment capable of being used in different places, e.g., a portable automobile phone.

Prior art

Portable automobile phones are used in the sate of being installed in automobiles (hereinafter, referred to as a car-installed state) in some cases and are used in the state of being carried by hand (hereinafter, referred to as a portable state) in the other cases. An automobile phone generally includes a

volume control circuit for optimizing the volume of a call in both of the car-installed state and the portable state depending on use conditions. More specifically, in the car-installed state, the volume is turned up because the environmental noise level is high. On the other hand, in the portable state, the volume is turned down because the environmental noise level is low. However, conventional volume control circuits need volume adjustment at every change of the use condition as described above. Accordingly, a large number of tasks are needed in a call and therefore phones have poor usability.

In view of such circumstances, it is an object of the present invention to provide a volume control circuit having excellent usability.

It is another object of the present invention to provide a volume control circuit that does not need volume adjustment at every change of the use condition of equipment.

CLAIMS

1. A volume control circuit comprising:

amplifying means for amplifying an audio signal;

first and second holding means for holding a gain of the amplifying means at a first value and a second value, respectively;

condition detecting means for detecting a use condition of a device in which a volume control circuit is installed and

for outputting a condition detection signal; and

switching means for allowing one of the first and second holding means to operate, in response to the condition detection signal.

2. The volume control circuit of claim 1, further comprising setting means for selectively changing the first and second setting values of the respective first and second holding means in response to the condition detection signal.

3. A volume control method comprising the steps of:

holding a plurality of amplification factors respectively associated with a plurality of use conditions of a device;

detecting one of the plurality of use conditions and outputting a condition detection signal; and

selecting, in response to the condition detection signal, one of the amplification factors associated with the condition detection signal and amplifying an audio signal.

4. The volume control method of claim 3, further comprising the step of manually changing the plurality of amplification factors.

（問２）

Hereinafter, operation of this pulse detecting circuit will be described. When a clock pulse to the input terminal CLK changes to the Vdd level, the FETs T3 and T5 are turned off and the FETs T4 and T6 are turned on. Accordingly, the Vss level is applied across both ends of the capacitor C3. When the clock pulse changes to the Vss level, the FET T3 is turned on, so that the Vdd level is applied to one end of the capacitor C3. At this time, suppose the point D is at the Vss level, the substrate of the FET T5 is at the Vss level, so that the FET cannot be turned on as transistor operation. However, as the potential at this end of the capacitor C3 rises to the Vdd level, the potential at the other end of the capacitor C3 increases, so that the pn junction formed between the substrate and a region connected to the capacitor C3 in the FET T5 is biased in the forward direction. As a result, current flows via this pn junction and the capacitor C4 is charged. The potential rise at the point D due to the charging of the capacitor C4 causes the FET T5 to turn on by transistor operation and also causes current flowing via the capacitor C3 to flow in the source-drain channel of the FET T5. At this time, the electrode of the FET 3 connected to the capacitor C3 serves as source. Transition of the clock pulse to the Vss level causes the FETs T3 and T5 to turn off, so that the point D is charged to a level lower than the Vdd level.