第 39 回電気電子　問題・原文ファイル

★★★ ＜第 39 回知的財産翻訳検定試験【第 19 回英文和訳】＞ ★★★

≪電気・電子分野≫

【解答にあたっての注意】

１．問題の指示により、「翻訳課題」と「チェック課題」があります。翻訳課題では翻訳し、チェック課題では既存の訳文をチェックしてください。解答は別紙「解答ファイル」に記載してください。

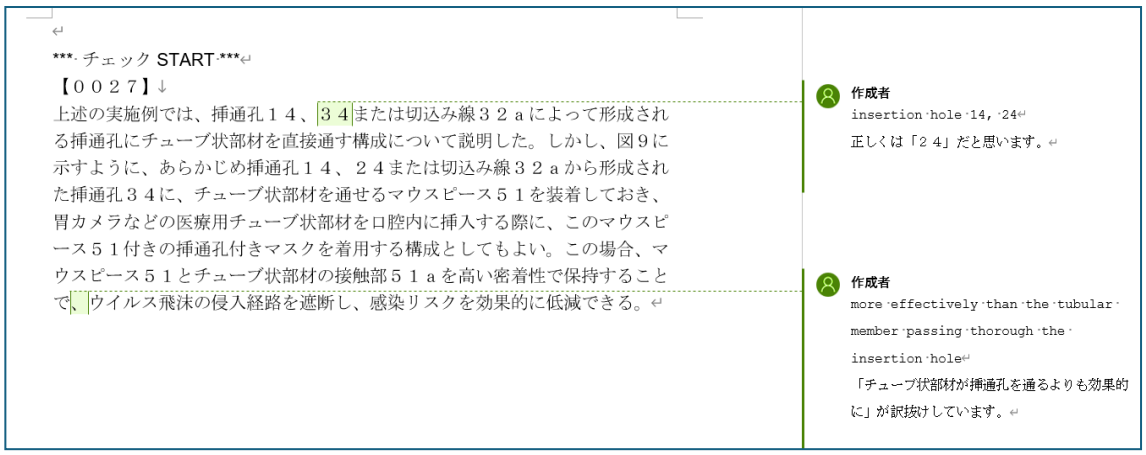
２．翻訳が求められる箇所は、*** 翻訳 START ***から*** 翻訳 END ***までの範囲です。

３．チェックが求められる箇所は、*** チェック START ***から*** チェック END ***までの範囲です。チェック対象の訳文は「解答ファイル」に記載されています。

４．チェック課題の解答方式

- 訳文の編集はせずに、訳文の不適切な箇所を指摘したうえで、正しい訳とその根拠を記載した「チェックコメント」を作成してください。

- チェックコメントの記載方式
  ①「解答ファイル」の該当箇所に Word コメント機能「吹き出し」で書く
  例：



  ②「解答ファイル」ではなく別途「チェックコメント」ファイルを作成しそちらに書く

  例：

受験番号：
氏名：
科目：機械工学

チェックコメント

問２
段落【００２７】
和訳の１行目「挿通孔１４、３４」
原文は「insertion hole 14, 24」ですので、「挿通孔１４、２４」の誤りだと思います。

問２
段落【００２７】
和訳の８行目
原文の「more effectively than the tubular member passing thorough the insertion hole」が訳抜けしています。「ウイルス飛沫の侵入経路を遮断し」の直前に「チューブ状部材が挿通孔を通るよりも効果的に」と入れるべきだと思います。

①②のどちらでも結構です。②の場合はファイル名を「チェックコメント（受験番号）」とし、対象箇所が分かるよう行や段落を明記してください。

５．全体の解答字数に特に制限はありません。適切な箇所で改行してください。

６．課題文に段落番号がある場合、これを訳文に記載してください。

７．設問は複数あります。それぞれの設問の指示に従い、すべて解答してください。

問１．以下の背景技術（流体搬送環境においてデータの収集、最適化等をおこなうための技術に関する発明）を和訳してください。

***** 翻訳 START *****

Heavy industrial environments, such as environments for large scale manufacturing (such as manufacturing of aircraft, ships, trucks, automobiles, and large industrial machines), energy production environments (such as oil and gas plants, renewable energy environments, and others), energy extraction environments (such as mining, drilling, and the like), construction environments (such as for construction of large buildings), and others, involve highly complex machines, devices and systems and highly complex workflows, in which operators must account for a host of parameters, metrics, and the like in order to optimize design, development, deployment, and operation of different technologies in order to improve overall results. Historically, data has been collected in heavy industrial environments by human beings using dedicated data collectors, often recording batches of specific sensor data on media, such as tape or a hard drive, for later analysis. Batches of data have historically been returned to a central office for analysis, such as undertaking signal processing or other analysis on the data collected by various sensors, after which analysis can be used as a basis for diagnosing problems in an environment and/or suggesting ways to improve operations. This work has historically taken place on a time scale of weeks or months, and has been directed to limited data sets.

The emergence of the Internet of Things (IoT) has made it possible to connect continuously to, and among, a much wider range of devices. Most such devices are consumer devices, such as lights, thermostats, and the like. More complex industrial environments remain more difficult, as the range of available data is often limited, and the complexity of dealing with data from multiple sensors makes it much more difficult to produce “smart” solutions that are effective for the industrial sector. A need exists for improved methods and systems for data collection in industrial environments, as well as for improved methods and systems for using collected data to provide improved monitoring, control, intelligent diagnosis of problems and intelligent optimization of operations in various heavy industrial environments.

Industrial system in various environments have a number of challenges to utilizing data from a multiplicity of sensors. Many industrial systems have a wide range of computing resources and network capabilities at a location at a given time, for example as parts of

the system are upgraded or replaced on varying time scales, as mobile equipment enters or leaves a location, and due to the capital costs and risks of upgrading equipment.

***** 翻訳 END *****

問２．以下の実施の形態（FPGA（Field Programmable Gate Array）に関する発明）を、英文に忠実に訳文チェックしてください。

[0054] FIG. 2 is a schematic block diagram of an exemplary TLFPGA (threshold logic FPGA) 22 according to embodiments described herein. The TLFPGA 22 is an integrated circuit (IC) which includes an array of TLFPGA logic tiles 24. As described further below with respect to FIGS. 3A and 3B, each TLFPGA logic tile 24 includes one or more programmable TLCs, as well as programmable interconnections between the TLFPGA logic tiles 24. An array of input/output (I/O) blocks 26 provides connection for field programmability and operation of the TLFPGA 22.

[0055] The exemplary TLFPGA 22 in this embodiment includes one or more memory blocks 28, which can include volatile memory (e.g., read-only memory (ROM), flash memory, dynamic random access memory (DRAM), synchronous DRAM (SDRAM), etc.) and/or non-volatile memory (e.g., flash memory, SRAM, etc.). The memory blocks 28 may store instructions, inputs, results, and so on in accordance with the configuration of the TLFPGA 22.

[0056] In some examples, the TLFPGA 22 may optionally include one or more additional processor blocks 30, which may be digital signal processor (DSP) blocks, discrete gate or transistor logic, discrete hardware components, or any combination thereof designed to perform functions of the TLFPGA 22. In some examples, the processor blocks 30 are also field-programmable in a manner similar to the TLFPGA logic tiles 24.

[0057] FIG. 3A is a schematic diagram of an exemplary TLFPGA logic tile 24 for the TLFPGA 22 of FIG. 2. Similar to the traditional FPGA logic tile 10 of FIGS. 1A and 1B, the TLFPGA logic tile 24 includes a programmable BLE block 12, as well as configuration registers 14 and intra-tile interconnect resources 16 (e.g., a set of MUXs) which are used to program the BLE block 12. However, the TLFPGA 22 uses a novel logic tile architecture where the BLE block 12 includes one or more TLCs 32. In an exemplary aspect, the BLE block 12 includes a cluster of LUT-Ks 18 and TLCs 32. In the TLFPGA logic tile 24 of FIG. 3A, the BLE block 12 includes three LUT-Ks 18 and one TLC 32. In some examples, the BLE block 12 can be referred to as an adaptive logic module (ALM) block, where the LUT-Ks 18 and TLCs 32 are referred to as ALMs.

[0058] Both LUT-Ks 18 and TLCs 32 are BLEs capable of implementing Boolean functions. Compared to a standard LUT cell, the proposed TLC 32 has smaller overall

delay, area and power consumption when implementing the same function. The TLFPGA implementation shows significant improvement in area and power without sacrificing performance, as compared to the traditional FPGA implementation of FIGS. 1A and 1B. The TLFPGA logic tile 24 further includes inter-tile interconnect resources 20 (e.g., MUXs and/or switches).

[0059] FIG. 3B is a schematic diagram of an alternative TLFPGA logic tile 24 for the TLFPGA 22 of FIG. 2. In the TLFPGA logic tile 24 of FIG. 3B, the BLE block 12 includes eight LUT-Ks 18 and two TLCs 32.

[0060] With continuing reference to FIGS. 3A and 3B, the TLC 32 is a digital CMOS circuit implementation of a binary perceptron, whose function is referred to as a threshold function or a linearly separable function. A unate Boolean function f (x1, x2, ..., xn) is called a threshold function if there exist weights wi for i = 1, 2, ..., n and a threshold T such that:

$f(x_1, x_2, ..., x_n) = 1 \leftrightarrow \Sigma_{i=1}^{n} w_i x_i \geq T$ Equation 1

where E denotes the arithmetic sum. Thus a threshold function can be represented as $(W,T)=[w_1, w_2, ..., w_n; T]$. An example of a simple threshold function is f (a, b, c, d)=abc v abd with $[w_1, w_2, w_3, w_4; T]=[2,2,1,1; 5]$. A more complex threshold function is g(a, b, c, d, e)=ab v acd v bcd v ace v bce v ade v bde with $[w_1, w_2, w_3, w_4, w_5; T]=[2,2,1,1,1; 4]$. Although threshold functions can be implemented as static CMOS logic circuits, implementations that are based on evaluating the defining predicate in Equation 1 by comparing some physical quantity such as charge or conductance can result in substantial reductions in gate count, area and power, as well as improving the performance when compared to standard logic implementations.

*** チェック **START** ***

[0061] FIG. 4 is a schematic diagram of a transistor-level structure of an embodiment of the TLC 32 of FIGS. 3A and 3B. The TLC 32 includes a sense amplifier 34, a latch 36, a left input network 38, and a right input network 40. The TLC 32 circuit operates in two phases. In the reset phase (CLK=0), N5 and N6 are discharged, turning off all discharge paths from N1 and N2 to ground. The outputs N1 and N2 transition to logic high (e.g., 1) through M1 and M4.

[0062] Evaluation takes place when CLK:0→1, assuming that the inputs have arrived, and that the left input network 38 has higher conductivity than the right input network 40. In the evaluation phase, M13 and M14 are turned OFF, and both N5 and N6 will rise to logic high. Without the loss of generality, assume as a result, node N5 rises before node N6, and turns M7 on. Prior to evaluation, N1 and N2 were both logic high. Hence, M5 is active when M7 turns on. This discharges N1 through M5 and M7. The discharge of N1 stops the further discharge of N2 by turning off M6 and turning on M3. Consequently, the final values of the outputs are N1=0, N2=1, which resets the output latch 36.

[0063] If the right input network 40 had high conductivity, the result would have been N1=1, N2=0, which results in setting the latch 36. Note the feedback involving M9 and M10. These are strictly unnecessary but are included to ensure that once the clock transition completes, further changes on the inputs will not affect the outputs.

[0064] The signals applied to the left input network 38 and right input network 40 are complementary, to ensure that there will always be a difference of at least one active transistor between the two networks. A configuration register R_i=0 if input X_1 is to appear in positive polarity, and R_i=1 if X_1 is to be complemented. The use of complementary signals in the two input networks ensures a strict inequality between the conductivity of the left input network 38 and the right input network 40 and prevents the sense amplifier 34 from being in a metastable condition.

***** チェック END *****

[0065] For the TLC 32 to properly realize a threshold function, the predicate shown in Equation 1 has to be converted to a strict inequality, and the variables in Equation 1 have to be mapped to its inputs. Thus, Equation 1 is replaced with $\Sigma_{i=1}^{n} 2w_i x_i > 2T-1$. As the signals driving the input networks 38, 40 are complementary, to realize this inequality the same number of literals representing a signal must appear in both networks. For example, consider f(a,b,c)=a V bc≡2a+b+c≥2≡4a+2 b+2c>3. This is rewritten as 2a+b+c+1>2(1−a)+(1−b)+(1−c). Therefore the signals assigned to left input network 38 in FIG. 2 would be X_1=a, X_2=a, X_3=b, X_4=c, X_5=1, X_6=0, and X_7=0, and R_i=1 for i=1, 2, ..., 7.

（参考図面）

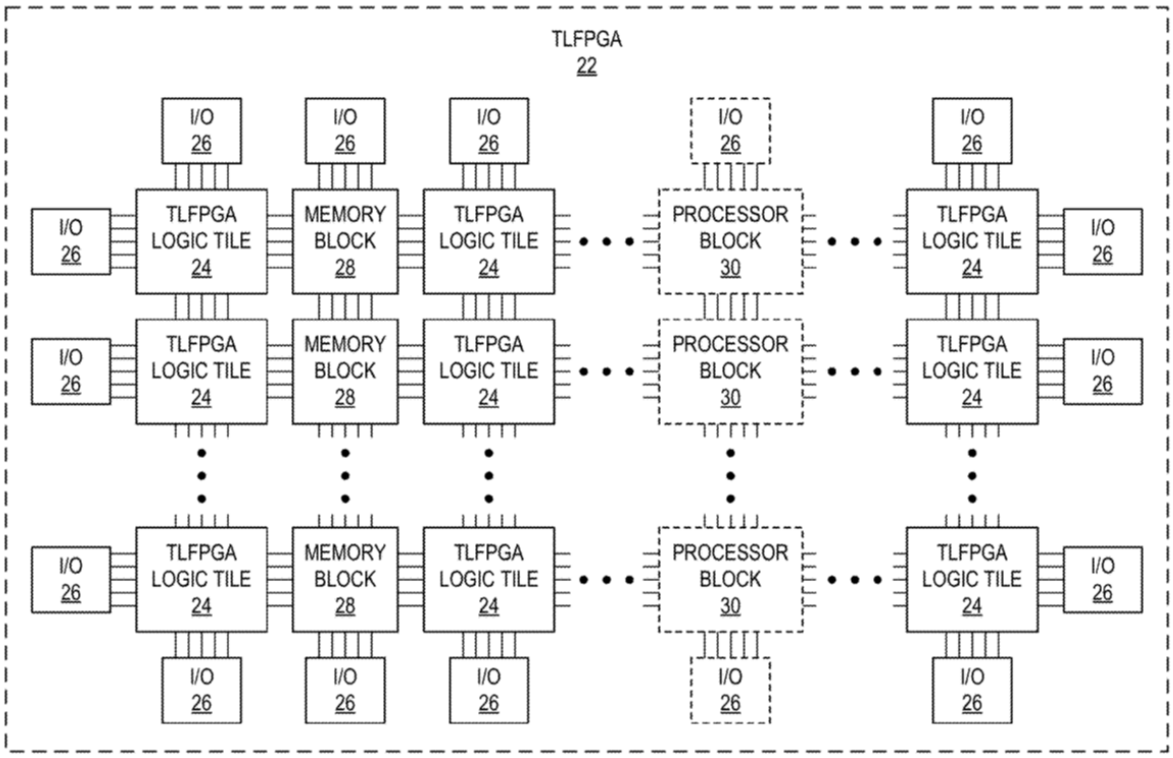

TLFPGA
22
I/O
26
TLFPGA
LOGIC TILE
24
MEMORY
BLOCK
28
PROCESSOR
BLOCK
30

FIG. 2

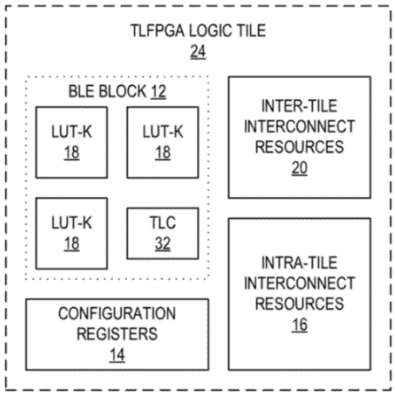


FIG. 3A

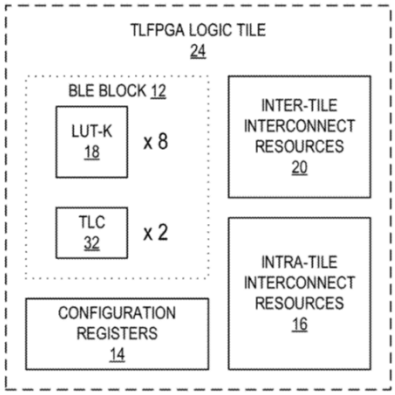


FIG. 3B

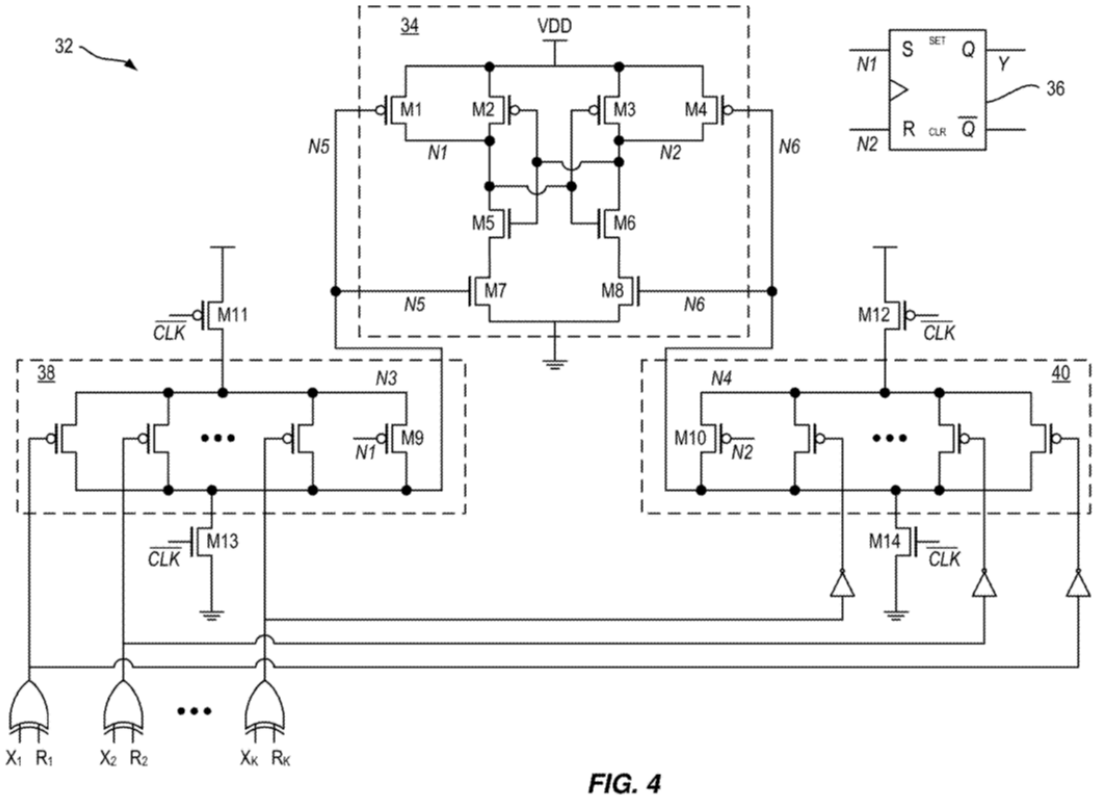


FIG. 4

問３．以下の請求項１（磁場に敏感な部品の動作に影響することなく非接触で充電する技術に関する発明）を翻訳してください。なお、この問題文が記載されている米国特許公報は US 12,400,779 B1 ですので、技術理解の援用に適宜ご参照ください。

***** 翻訳 START *****

1. An inductive charger for inductive charging a battery in an electronic device having a substantially planar receiver coil, the inductive charger comprising:

a substantially planar inductive charger coil comprising Litz wire wound in a substantially spiral shape for generating an alternating magnetic field substantially perpendicular to the plane of the inductive charger coil to transfer inductive power to the receiver coil in the electronic device for charging the battery in the electronic device;

a magnetic structure configured to generate a magnetic field that creates a magnetic attachment between the inductive charger and the electronic device and to align the inductive charger coil with the receiver coil of the electronic device for inductive power transfer for charging the battery in the electronic device, the magnetic structure comprising two or more discontinuous arc-shaped permanent magnet sections that define a substantially flat first surface and a substantially flat second surface opposite the first surface,

wherein each magnetic section comprises at least two magnetic poles of opposite polarity located at each of the first and second surfaces of each magnetic section such that each magnetic section includes at least two pairs of opposing magnetic poles oriented to cause magnetization in two opposing directions that are each perpendicular to the first and second surfaces,

wherein the magnetic sections are assembled to form a full or partial ring shape and the magnetic structure is positioned around an outer perimeter of the inductive charger coil and is substantially concentric with the inductive charger coil, and

wherein the magnetic structure is configured to create a magnetic field with flux densities having substantially similar magnitudes relative to the first and second surfaces as a function of distance from the first and second surfaces, respectively, along an axis that runs perpendicular to the first and second surfaces; and

a magnetic shield layer comprising a nano-crystalline material positioned parallel to the plane of the inductive charger coil on a side of the inductive charger coil that is opposite the electronic device during inductive power transfer,

wherein the magnetic shield layer is positioned to shield a portion of the inductive charger from the alternating magnetic field while transferring the inductive power;

wherein the magnetic structure is configured such that:

the magnetic field generated by the magnetic structure does not impair operation of the magnetic shield layer during the inductive power transfer, and

the electronic device can be rotated across a continuous range of rotational angles with respect to the inductive charger while keeping the alignment between the inductive charger coil and the inductive receiver coil during inductive power transfer for charging the battery in the electronic device.

***** 翻訳 END *****